

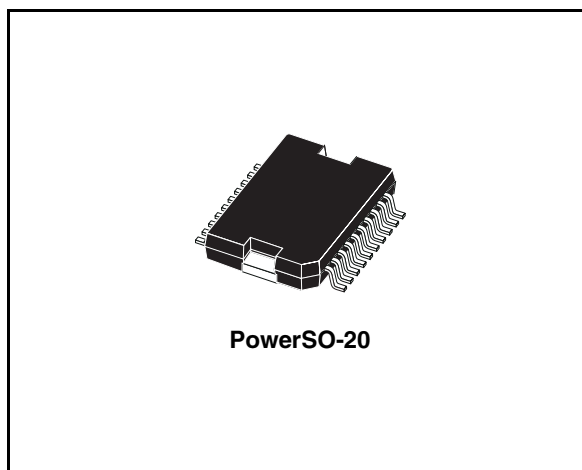
## 32 W bridge car radio amplifier

### Features

- High power capability:
  - 40 W/3.2  $\Omega$  EIAJ
  - 32 W/3.2  $\Omega$  @  $V_S = 14.4$  V,  $f = 1$  kHz,  $d = 10$  %
  - 26 W/4  $\Omega$  @  $V_S = 14.4$  V,  $f = 1$  kHz,  $d = 10$  %
- Differential inputs (either single ended or differential input signal are accepted)
- Minimum external component count:
  - No bootstrap capacitors
  - No Boucherot cells
  - Internally fixed gain (30 dB)
  - No SVR capacitor
- Stand-by function (CMOS compatible)
- Programmable turn-on/off delay
- No audible pop during mute and stand-by operations

### Protections

- Short circuit (to GND, to  $V_S$ , across the load)
- Very inductive loads
- Chip over temperature
- Load dump
- Open GND
- ESD



### Description

The TDA7391PD is a bridge class AB audio power amplifier specially intended for car radio high power applications.

The high power capability together with the possibility to operate either in differential input mode or single ended input mode makes it suitable for boosters and high end car radio equipment. The exclusive fully complementary output stage and the internal fixed gain configuration drop the external component count.

The on board clipping detector allows easy implementation of gain compression systems.

**Table 1. Device summary**

Order code	Package	Packing
TDA7391PD	PowerSO-20	Tube
TDA7391PD13TR	PowerSO-20	Tape and reel

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# 1 Test and application circuit, block diagram

Figure 1. Test and application circuit

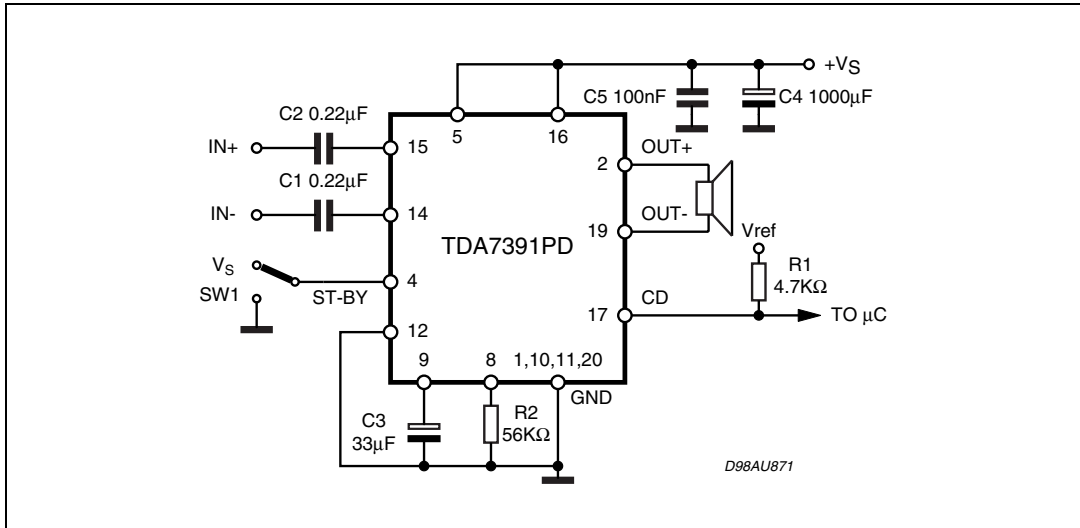
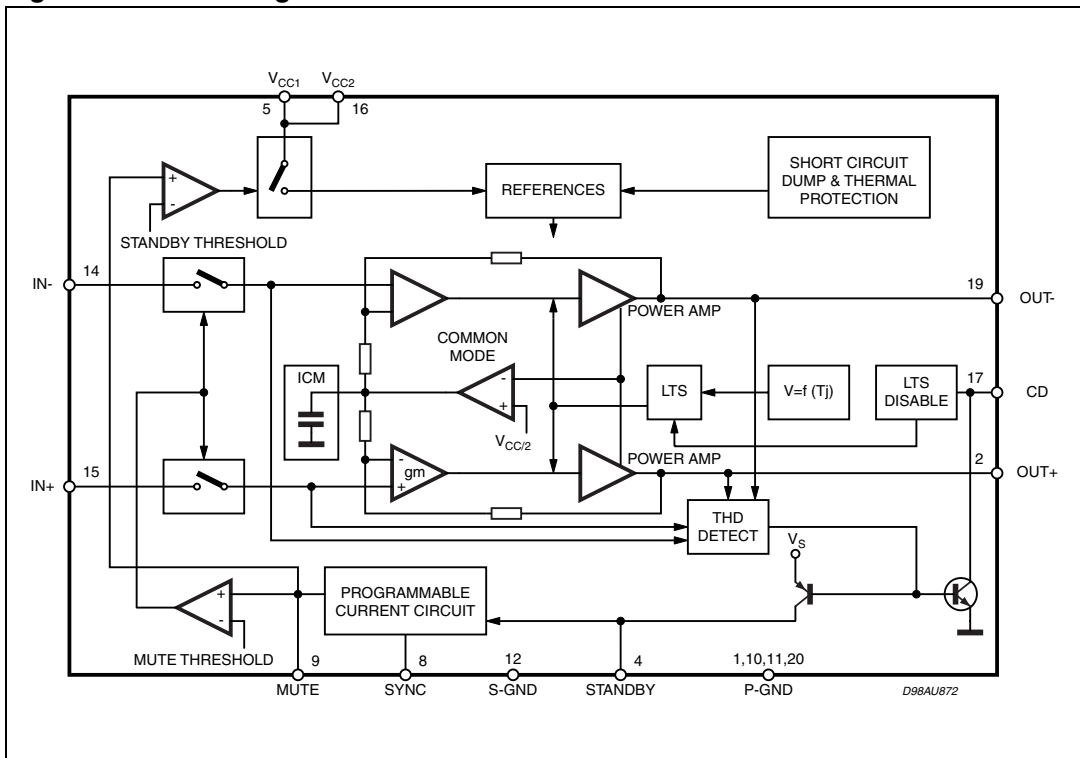


Figure 2. Block diagram



## 2 Pins description

Figure 3. Pins connection (top view)

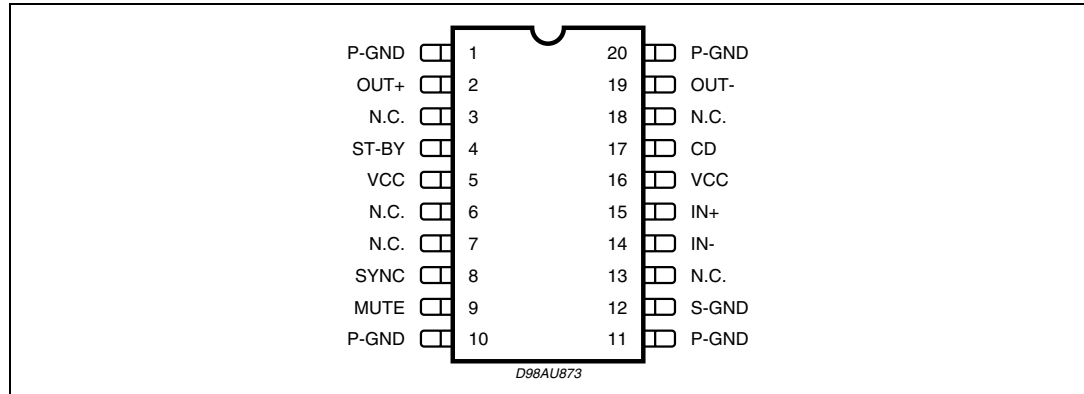


Table 2. Pins function

Pin	Function	Description
14, 15	INPUTS	The input stage is a high impedance type also capable of operation in single ended mode with one input capacitively coupled to the signal GND. The impedance seen by the inverting and non inverting input pins must be matched.
5, 16	+V <sub>S</sub>	Supply voltage.
17	CD	The TDA7391PD is equipped with a diagnostic circuitry able to detect the clipping in the Output Signal (distortion = 10%). The CD pin (open collector) gives out low level signal during clipping.
2, 19	OUTPUTS	The output stage is a bridge type able to drive loads as low as 3.2Ω. It consists of two class AB fully complementary PNP/NPN stages fully protected. A rail to rail output voltage swing is achieved without need of bootstrap capacitors. No external compensation is necessary.
1, 10, 11, 20	GND	Power Ground.
12	S-GND	Signal ground.
4	STAND-BY	The device features a ST-BY function which shuts down all the internal bias supplies when the ST-BY pin is low. In ST-BY mode the amplifier sinks a small current (in the range of few μA). When the ST-BY pin is high the IC becomes fully operational.
8	SYNC	A resistor (R <sub>2</sub> ) has to be connect between pin 8 and GND in order to program the current that flows in the C <sub>3</sub> capacitor (pin 9). The values of C <sub>3</sub> and R <sub>2</sub> determine the time required to bias the amplifier.
9	MUTE	The pin will have a capacitor (C <sub>3</sub> ) tied to GND to set the MUTE/STAND-BY time. An automatic Mute during turn on/off is provided to prevent noisy transients.

## 3 Electrical specifications

### 3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_S$	DC supply voltage	28	V
$V_{OP}$	Operating supply voltage	18	V
$V_{PEAK}$	Peak supply voltage (t = 50 ms)	50	V
$I_O$	Output peak current repetitive (f > 10 Hz)	4.5	A
	Output peak current non repetitive	6	A
$P_{tot}$	Power dissipation ( $T_{case} = 85\text{ }^\circ\text{C}$ )	32	W
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

### 3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal resistance junction to case	Max. 2	$^\circ\text{C/W}$

### 3.3 Electrical characteristics

Table 5. Electrical characteristics

( $V_S = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ , f = 1 kHz,  $T_{amb} = 25\text{ }^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_S$	Supply voltage range		8		18	V
$I_q$	Total quiescent current			60	150	mA
$V_{OS}$	Output offset voltage				120	mV
$I_{SB}$	St-by current	$V_{ST-BY} = 1.5\text{ V}$			100	$\mu\text{A}$
$I_{SBin}$	St-by input Bias current	$V_{ST-BY} = 5\text{ V}$			10	$\mu\text{A}$
$V_{SBon}$	St-by on threshold voltage				1.5	V
$V_{SBoff}$	St-by off threshold voltage		3.5			V
$ATT_{ST-BY}$	St-by attenuation			90		dB
$I_{M\ in}$	Mute input bias current	( $V_{MUTE} = 5\text{ V}$ )			10	$\mu\text{A}$
$A_M$	Mute attenuation			90		dB

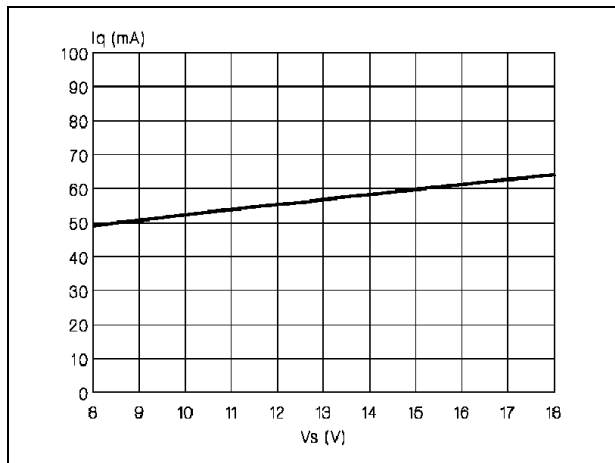
**Table 5. Electrical characteristics (continued)**

( $V_S = 14.4\text{ V}$ ;  $R_L = 4\ \Omega$ ,  $f = 1\text{ kHz}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ , unless otherwise specified)

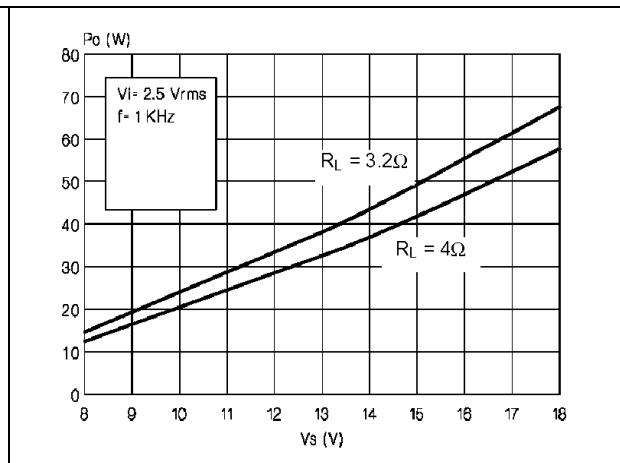
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$P_O$	Output power	$d = 10\%$	20	26		W
		$d = 1\%$		21		W
		$d = 10\%$ ; $R_L = 3.2\ \Omega$		32		W
$P_{O\ EIAJ}$	EIAJ output power (*)	$V_S = 13.7\text{ V}$		40		W
$d$	Distortion			0.06		%
		$P_O = 0.1\text{ to }15\text{ W}$		0.03		%
$G_V$	Voltage gain		29.5	30	30.5	dB
$f_H$	High frequency rolloff	$P_O = 1\text{ W}$ ; $-3\text{ dB}$	75			KHz
$R_{IN}$	Input Impedance	Differential	36	60		$K\Omega$
		Single Ended	30	55		$K\Omega$
$E_{IN}$	Input noise voltage	$R_g = 0\ \Omega$ ; $f = 22\text{ Hz to }22\text{ kHz}$		4		mV
CMRR	Input common mode rejection	$f = 1\text{ kHz}$ ; $V_{IN} = 1\text{ V}_{rms}$		65		dB
SVR	Supply Voltage Rejection	$R_g = 0\ \Omega$ ; $V_r = 1\text{ V}_{rms}$		60		dB
CDL	Clipping Detection Level			10		%
$T_{sd}$	Absolute Thermal Shutdown Junction Temperature			160		$^\circ\text{C}$

### 3.4 Electrical characteristics curves

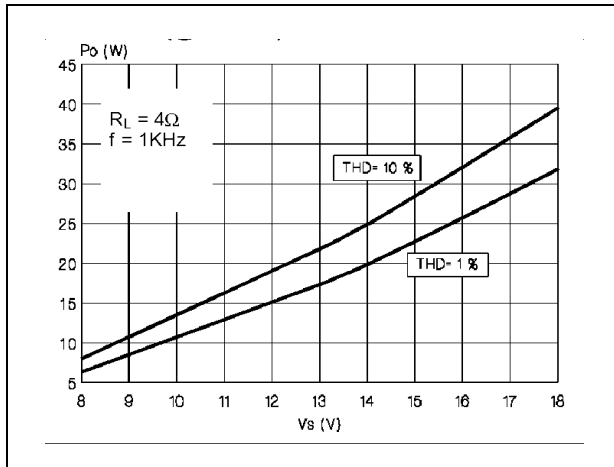
**Figure 4. Quiescent current vs. supply voltage**



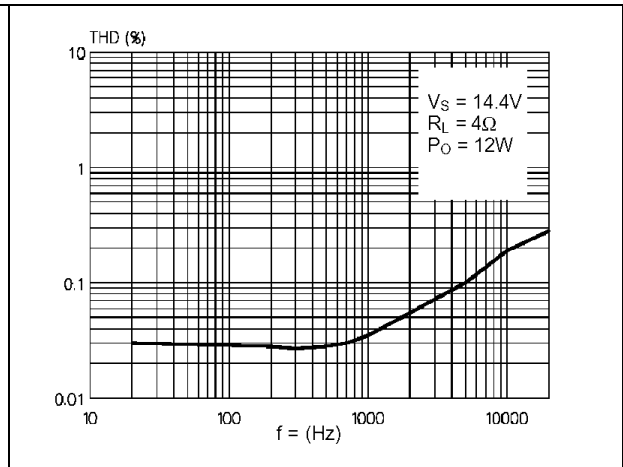
**Figure 5. EIAJ power vs. supply voltage**



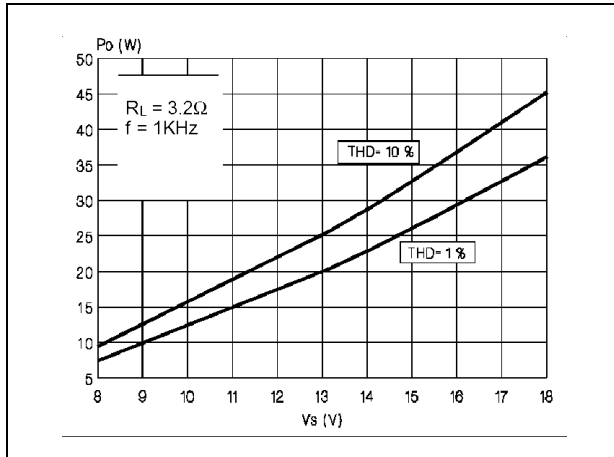
**Figure 6. Output power vs. supply voltage (@ $R_L = 4\Omega$ )**



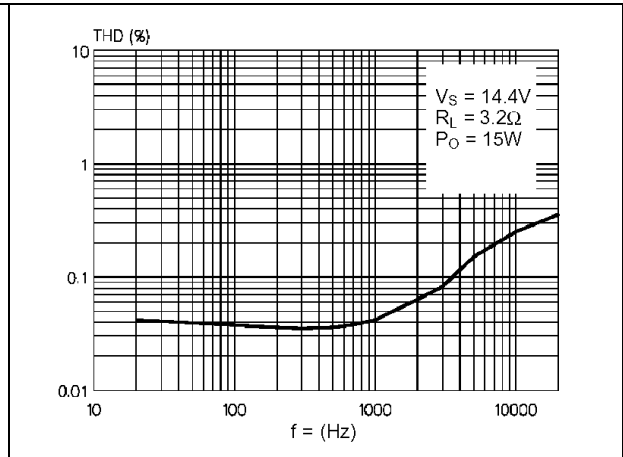
**Figure 7. Distortion vs. frequency (@  $R_L = 4\Omega$ )**



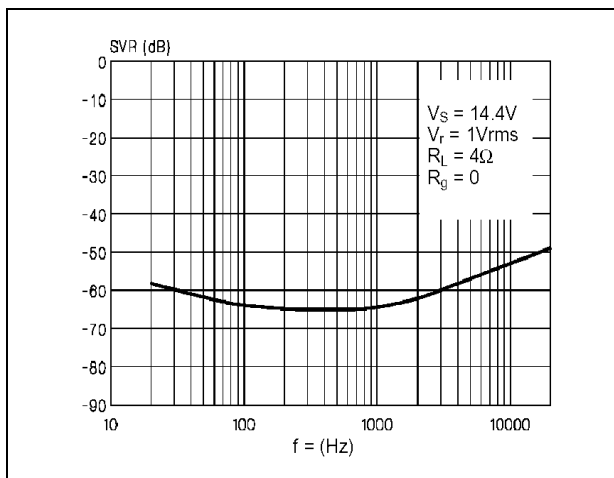
**Figure 8. Output power vs. supply voltage (@ $R_L = 3.2\Omega$ )**



**Figure 9. Distortion vs. frequency (@  $R_L = 3.2\Omega$ )**



**Figure 10. Supply voltage rejection vs. frequency**



**Figure 11. Common mode rejection vs. frequency**

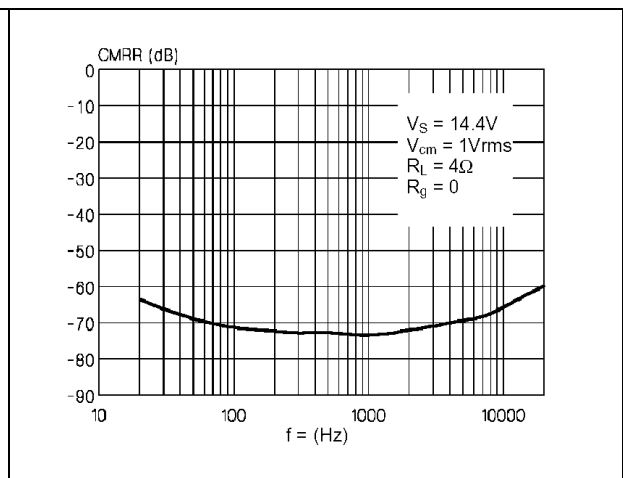


Figure 12. Total power dissipation and eff. vs. output power (@ $R_L = 4\Omega$ )

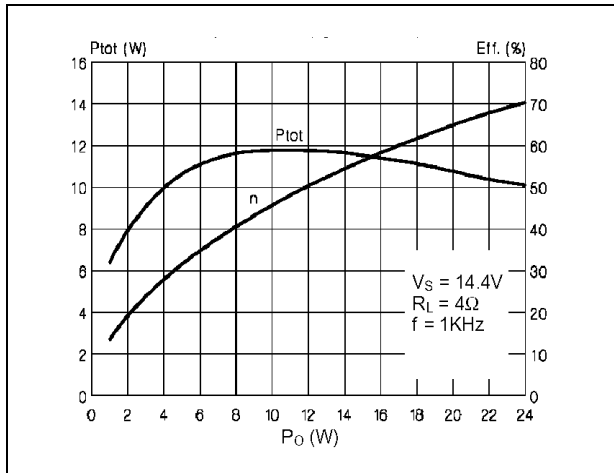
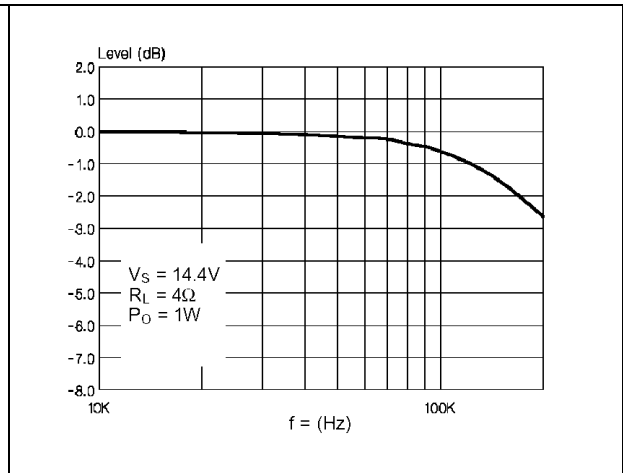


Figure 13. Power bandwidth



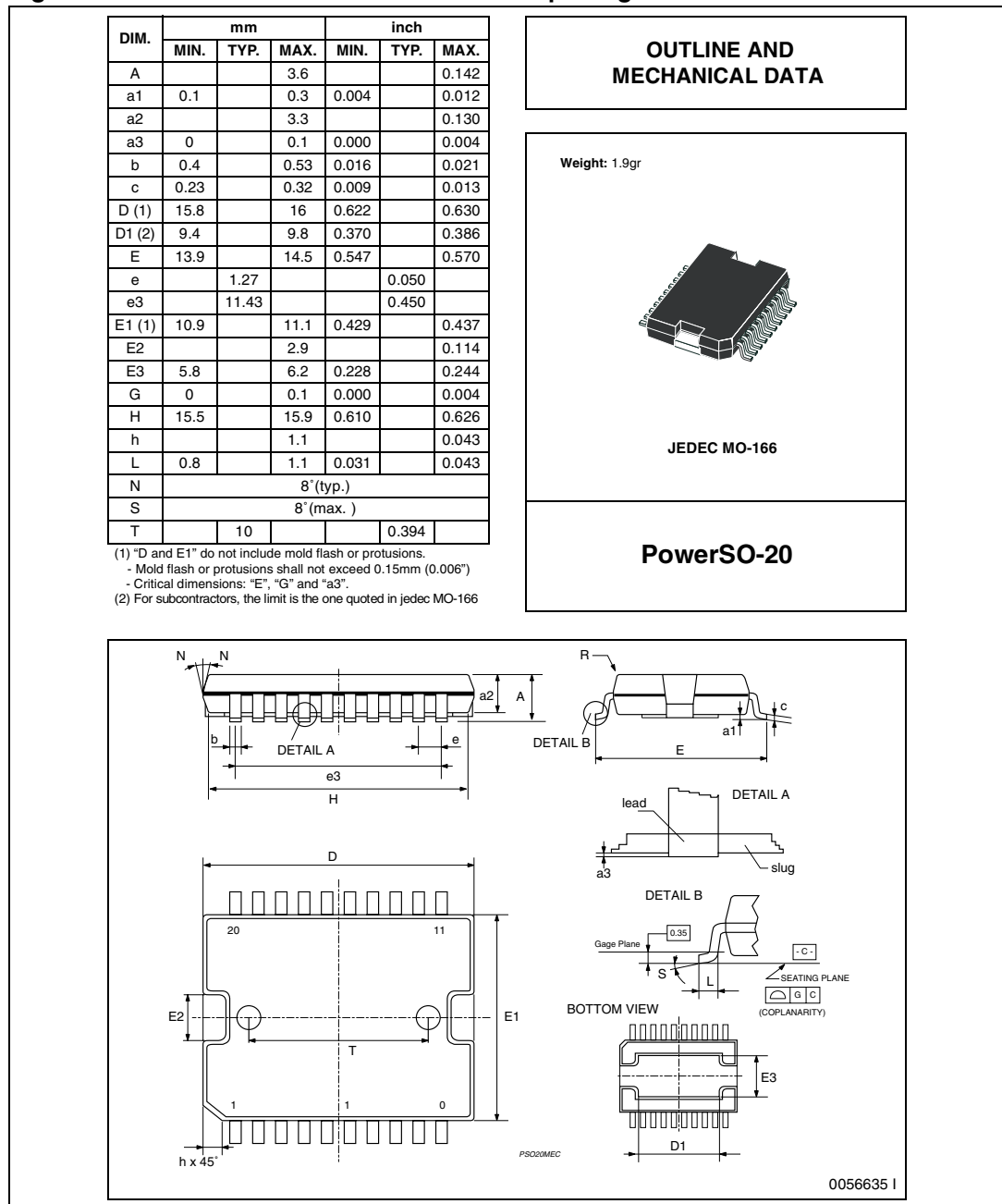


# 4 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

**Figure 14. PowerSO-20 mechanical data and package dimensions**



## 5 Revision history

**Table 6. Document revision history**

Date	Revision	Changes
10-Oct-1998	1	Initial release.
02-Jul-2008	2	Document reformatted. Document status promoted from product preview to datasheet. Added <a href="#">Table 1: Device summary</a> . Added ECOPACK description in <a href="#">Section 4: Package information</a> .

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